A Comparative Analysis of Two Approaches in Envelope Tracking Power Supplies for Satellite Applications

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***Abstract*—In modern telecommunication systems, the requirements for amount of transmitted data are increasing. In order to transmit as much information as possible for a given spectral band, both amplitude and phase modulation are applied. The main power consumers in transmitters are power amplifiers (PA), placed in the output stage. During the last decade, a lot of efforts have been invested in optimization of the efficiency of RF power amplifiers. One of notable techniques is Kahn's envelope and restoration (EER) principle, where highly efficient envelope tracker and non-linear RF amplifier (e.g. class E, F) are combined. In this paper, two different approaches in envelope tracking are presented. The first approach is based on an analog multiplexer and a linear regulator in series, while the second tracker consists of PWM controlled switches and the fourth order output filter. Both trackers are supplied with highly efficient (96%) switch-capacitor based multilevel power converter, which acts as a voltage divider. Additionally, the comparison between two prototypes of the first approach, with Si and GaN based transistors is presented. Experimental results show that peak efficiencies are 73% (Si) and 75% (GaN), in the case of a 5 MHz 64QAM reference signal, with 10 W average output power. For the second approach, different filter prototypes are analysed. Moreover, their impact on envelope signal processing is backed up with the simulation results and the experimental results for tracking of a 2 MHz 64QAM reference are presented, with 78% achieved efficiency (Si technology) and 9 W average output power.**

I. Introduction

In modern telecommunication systems, the requirements for transmitted data are increasing. To improve the spectral efficiency of the transmitted signal, both amplitude and phase modulations are employed. The spectral bandwidth and the peak-to average power ratio (PAPR) have big values. Power amplifiers, which are obligatory part of the output stage of transmitters, suffer from low efficiency, especially if conventional amplifiers are used (class A, AB or B). These amplifiers have good linearity, but poor efficiency for the required conditions. About sixty years ago, Kahn proposed elimination and restoration (EER) principle, where amplitude and phase of transmitted signal were processed separately [2]. During the last decade, several techniques were the subject of research: EER, ET (Envelope Tracking), Doherty technique, and so on [5]. In this paper, EER technique will be used. The important part of the scheme from Figure 1 is DC/DC converter, called envelope amplifier (or envelope tracker). The aim of this converter is to amplify the envelope of the input RF signal. The amplified signal will serve as voltage supply for highly efficient power amplifier (class E or F), which is processing phase signal information. In that way, there is amplified RF signal at the output of power amplifier.

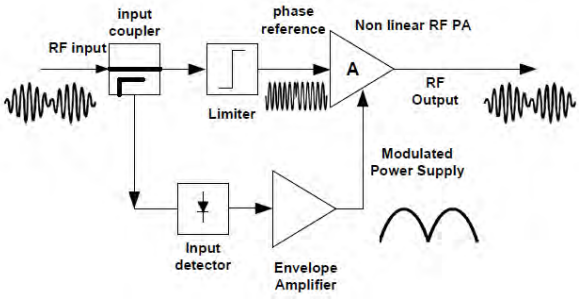

Fig. 1. Kahn's EER technique.

The main problem of envelope trackers is dynamics of DC/DC converter. They must be able to provide accurate tracking of the envelope reference with high efficiency, which can allow reduced volume design due to thermal issues, and also low weight. These requirements are mandatory for satellite applications.

Here are presented two approaches in the design of envelope trackers. The same part of both envelope trackers is switched-capacitor based, multilevel voltage supply. The optimization process of this multilevel converter is explained in details in [8]. In the first approach, envelope tracker is consisted of analog multiplexer with linear regulator in series, while the second approach is based on the five input buck converter (four voltage levels from multilevel converter and zero voltage) with high frequency PWM switching and fourth order output filter. Additionally, two different prototypes are fabricated: with GaN and Si based transistor. It will be shown and with experimental results verified, that this approach offers high

accuracy and good efficiency, especially with GaN transistors. The second approach is verified at simulation level and with experimental results, comparing different filter prototypes and their impact on the converter efficiency and the quality of processed 64QAM signal. In both cases, power amplifier is modelled with linear time-invariant resistor.

II. Proposed Solutions

A. General idea

The essence of the both approaches is switching structure, whose role is to select an appropriate voltage level. This structure is called analog multiplexer. The rest of the circuits differ from linear regulator, in the first proposal, and the passive filter, in the second proposal. These two systems are shown in Figure 2 and 3, respectively. It is assumed that multilevel voltage level generation can be obtained from an outer voltage divider.

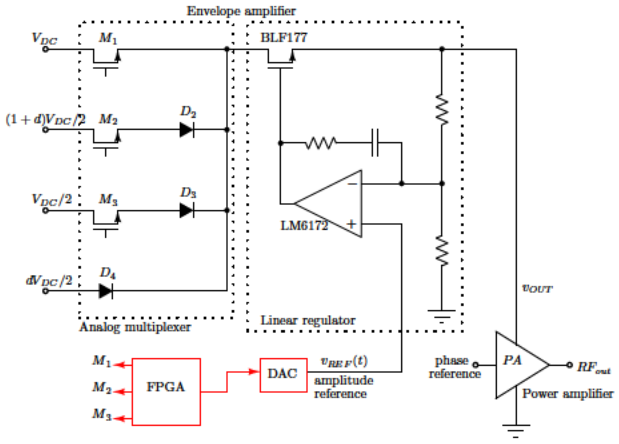

Fig. 2. Linear assisted envelope tracker.

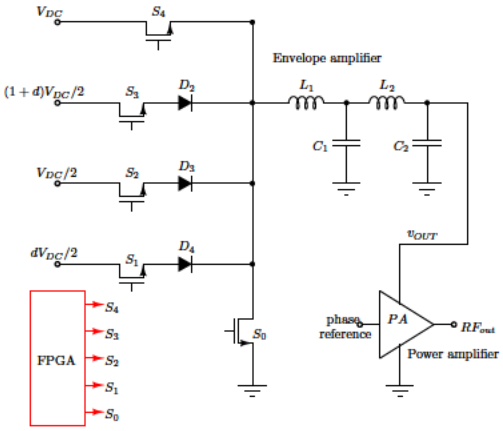

Fig. 3. Five level buck converter with fourth-order output filter.

B. Multilevel converter

One of the key points for both approaches is multilevel voltage input. Both envelope trackers are supplied with a set of voltage levels. That is provided using a switched-capacitor based, multilevel converter which operates as voltage divider as shown in Figure 4. Flying capacitor C_{fly} is placed between two switching nodes in order to maintain middle voltage to be half of the input voltage V_{DC}. Two buck type structure consists of transistors S_1, S_2 and S_3, S_4 produce pulsating voltage between $V_{DC} - V_{DC}/2$ and $V_{DC}/2 -$ ground, in the two switching nodes. These pulsating voltages are filtered by LC output filters, providing stable output voltages $(1+d)\,V_{DC}/2$ and $d\,V_{DC}/2$ at the output.

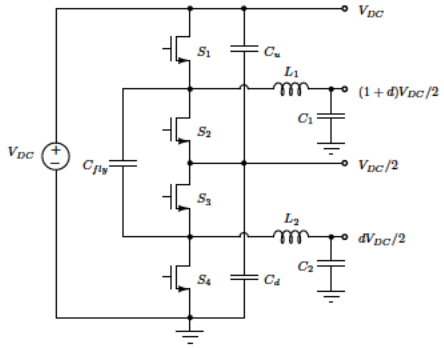

Fig. 4. Switched-capacitor multilevel converter.

The first advantage is the possibility to modulate two of its output voltages, by the means of duty-cycle d, which can be used in the optimization process of overall envelope tracker. The second advantage is the high efficiency, especially when GaN transistors are used. In GaN case, peak efficiency of this converter is around 96.15 % for the 5 MHz bandwidth of 64QAM signal. High efficiency is associated with low prototype volume, due to the thermal issues, also allowing low occupied space and low weight. Also, GaN based transistors are proved to have better resistivity on space radiations, compared with p-n junction based transistors. All these advantages make this converter convenient to use in satellite applications where all these benefits are mandatory.

C. Linear assisted envelope amplifier

Linear power supplies with series transistor are suitable due to its simplicity. As they act as common drain amplifiers, they provide high bandwidth and accurate tracking of reference voltage with low ripple, without produced noise. The main disadvantage of these power supplies is the fact that their efficiency depends on drain to source voltage of the series transistor, which is the difference between the supply voltage and the output voltage. Instead of constant supply voltage, multilevel voltage is used. Multilevel converter voltage should be close enough to the output voltage of the linear regulator, in order to decrease the voltage difference across the series transistor in the linear regulator. The proposed solution is shown in Figure 2.

For the mentioned purpose, the analog multiplexer is consisted of the switches that turn on and off the corresponding voltage level. MOSFET switches cannot block negative voltage and block diodes D_2 and D_3 are put in series with the transistors M_2 and M_3, respectively. The multiplexer

switching frequency is defined by reference envelope signal dynamics, the switching occurs when reference signal crosses certain threshold level [3]. The switching frequency is much lower than in the second proposed solution, where PWM multilevel converter is proposed.

The accurate control of the output voltage is achieved thanks to the control circuit with high-bandwidth operational (LM6172) in the linear regulator stage.

D. Five level buck converter

The main disadvantage of the previous approach is efficiency limitation caused by the linear regulator. Instead of using the linear regulator at the output of the envelope tracker, a low-pass filter can be employed, to mitigate the limitation problem. In that case, high switching frequency is needed to have smaller output filter. For example, in [1], two phase synchronous buck converter with fourth-order output filter is used. The advantage of that approach is absence of harmonics at the switching frequency and filter has to attenuate the harmonics at the twice of the switching frequency. The harmonics at the switching frequency can be smaller if modulated voltage at the filter input has smaller peak-to-peak variations. Instead of switching between maximum and zero voltage, switching operation can be distributed between several voltage levels. The schematic of the proposed system is shown in Figure 3. Input voltage levels are produces by multilevel voltage divider, presented in the previous chapter. Duty-cycle of the multilevel converter is chosen to be 0.5.

Being the reference signal v_{REF} presented with the set of digital values between 0 and 2^N-1 (N is the number of bits), being the maximum of carrier $N_C = \frac{2^N}{4} - 1$, as a result of the modulation process, designed as digital PWM in FPGA, averaged output voltage v_{OUT} is defined as follows, assuming the converter lossless:

$$v_{OUT} = \begin{cases} \dfrac{v_{REF}}{N_C} V_{DC}, & 0 \le v_{REF} < \dfrac{2^N}{4} - 1 \\ \dfrac{V_{DC}}{4} + \dfrac{v_{REF}}{N_C} V_{DC}, & \dfrac{2^N}{4} \le v_{REF} < \dfrac{2^N}{2} - 1 \\ \dfrac{V_{DC}}{2} + \dfrac{v_{REF}}{N_C} V_{DC}, & \dfrac{2^N}{2} \le v_{REF} < 3 \cdot \dfrac{2^N}{4} - 1 \\ \dfrac{3\,V_{DC}}{4} + \dfrac{v_{REF}}{N_C} V_{DC}, & 3 \cdot \dfrac{2^N}{4} \le v_{REF} \le 2^N - 1 \end{cases}$$

Due to the previous expression, the modulation process is divided into four sections. In each section, duty-cycle $d = \dfrac{v_{OUT}}{V_{DC}}$ has value from 0 to 1 and controls the pair of the corresponding transistors (S_0, S_1; S_1, S_2; and so on). Very small and very high values of duty-cycle can cause some problems, due to hardware restrictions, which will be seen in the next section.

The switching node voltage, that has to be filtered (Figure 5), has more favourable shape than in classical PWM modulation where two voltage levels are used. The lower amplitude of the high frequency harmonics, the lower values of inductors and capacitors in the output filter, in that way reducing the size and weight of converter, which is of crucial importance in satellite applications.

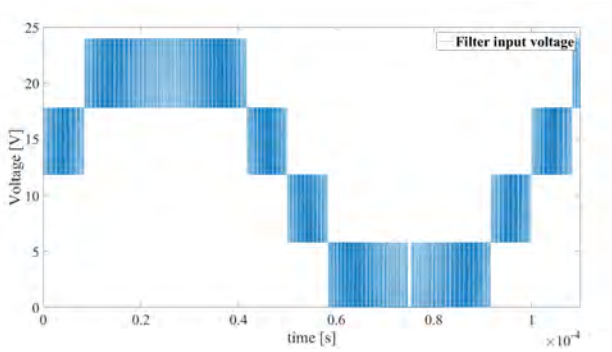

Fig. 5. The first version of the modulation process, for a sine reference.

Adding more dynamic elements in the converter, open-loop transfer function becomes more complicated, thus closed-loop control may be hard to design. Moreover, digital control would introduce additional delays which could cause bandwidth limitation and making the converter slower. However, due to the nature of converter switches, CCM of both inductors is warranted, so enabling linear relation between reference signal and the output voltage and converter can be driven in open-loop [7].

III. Design Considerations

A. Design of the Linear assisted envelope amplifier

Both prototypes with GaN (EPC2014) and Si transistors (FDMS7620S in the voltage divider, Si4840BDY in the analog multiplexer and VSSAF3L45-M3 diodes) for linear assisted switched-capacitor based envelope tracker are fabricated and verified. The photograph of the prototype with the multilevel converter dimensions is shown in Figure 6. The specifications are given as follows:

- Input DC voltage: $24\,\mathrm{V}$;
- Output voltage range: $0-24\,\mathrm{V}$;
- Peak output power: $40\,\mathrm{W}$;
- Average output power: $10\,\mathrm{W}$;
- PA emulated load (resistor): $15\,\Omega$;
- Maximum tracking frequency: $5\,\mathrm{MHz}$.

The prototypes for switched-capacitor based multilevel converter are designed and optimized following the process presented in [8].

All switches are controlled by FPGA signals. The envelope reference is saved in ROM memory and sent during the control process to a D/A converter and thus giving the reference for the linear regulator. The same reference is used in triggering logic for the switches. Having in mind that those two signals' paths (to the D/A converter and to switches) take different processing time and have different physical distances, a digital delay filter is implemented in FPGA in order to synchronise the multilevel output voltage with linear amplifier's reference.

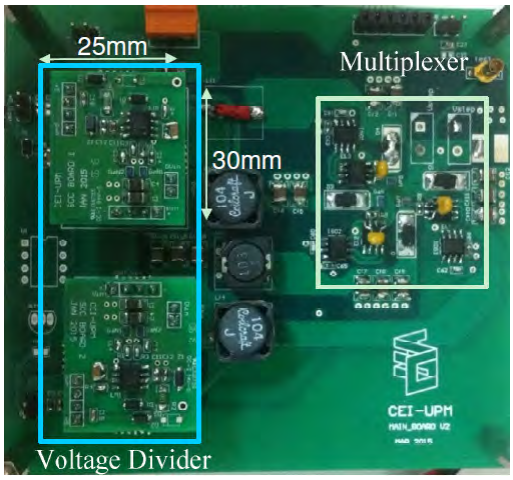

Fig. 6. Photograph of the implemented multilevel converter with analog multiplexer.

TABLE I
THE VALUES OF THE OUTPUT FILTER ELEMENTS

	L_1 [nH]	C_1 [nF]	L_2 [nH]	C_2 [pF]
Butterworth	702.74	3.22	496.93	780.88
Bessel	689.15	1.99	281.35	431.33
Legendre	740.07	3.39	656.15	1305.7

B. Design of the Five level buck converter

In the case when high frequency switching is used, an lossless passive output filter must be employed to filter out switching frequency information. The filter design is based on standard filter approximations with flat magnitude characteristics in pass-band, such as: Butterworth, Bessel, Legendre. Although pass-band ripple has negligible effect in these filter prototypes, bandwidth, group delays and switching frequency ripple have to be taken to account [6], [12]. The order of the filter for this type of applications is always even: it is a consisted of several LC sections. In this case, fourth order filter is chosen. For the given resistive load of $R = 15\,\Omega$ and cut-off frequency $f_C = 2\,(1+\beta)\,R_{sym} = 5.2\,\text{MHz}$, where $\beta = 0.3$ is roll-off factor and $R_{sym} = 2 \times 10^6\,\frac{\text{symbols}}{\text{s}}$ symbol rate of 64-QAM signal, the converter should operate at high switching frequency in order to have accurate envelope tracking. For the given symbol-rate, the switching frequency is preferable to be around 15 MHz or higher and thus switching losses would significantly decrease the converter efficiency. The values of filter elements for different filter approximations are given in Table I [9].

For the validation purpose and quantification the performance of the envelope tracker, the metrics based on three parameters is used: Error Vector Magnitude (EVM) and Adjacent Channel Power Ratio ($ACPR$) for left ($ACPR_L$) and right side ($ACPR_R$) band [11]. At the simulation level, using these metrics, Butterworth filter approximation based design has the best performance: $ACPR_L = 31.25$, $ACPR_R = 31.25$, $EVM = 4.71$. The constellation diagram of the ideal 2MHz 64QAM signal with simulated output signal for 15MHz switching frequency is shown in Figure 7, obtained by the simulation in Simplorer and Matlab.

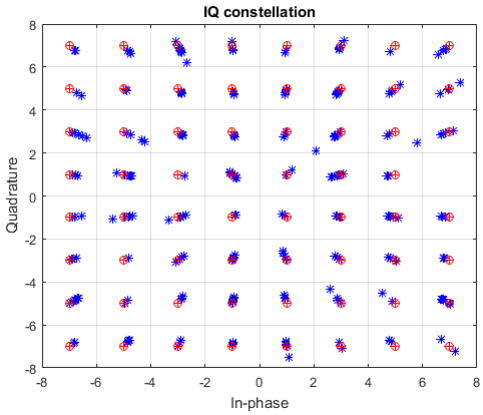

Fig. 7. Constellation diagram of ideal and simulated 2 MHz 64QAM signal.

This prototype is made using Si-based semiconductors (BSZ060NE2LS transistors and VSSAF3L45-M3 diodes), multilayer ceramic chip capacitors and air-core inductors (in the output filter). The photograph of the prototype is shown in Figure 8. The specifications are given as follows:

Fig. 8. Photograph of the implemented Five level buck converter with the voltage divider, the output filter and the FPGA board

- Input DC voltage: 24 V;
- Output voltage range: 0 – 24 V;
- Switching frequency: 15 MHz;
- Peak output power: 42 W;
- Average output power: 9 W;
- PA emulated load (resistor): 15 Ω;
- Maximum tracking frequency: 2 MHz.

All switches are controlled by FPGA signals. As previously mentioned, due to the modulation process, in some moments very low (or very high) value of the duty-cycle may be

required. The minimum pulse-width which can be provided by the hardware is 10 ns. This means that for the 15 MHz switching frequency, minimum duty-cycle is 15% (and 85%, maximum duty-cycle). In order to avoid additional distortions in the output voltage of this envelope tracker, a modification in the modulation process is made. In the critical region, where low/high value of duty-cycle is needed, switching operation is performed between two non-neighbour levels, so the resulting duty-cycle is around 50%, which can be seen in Figures 5 and 9.

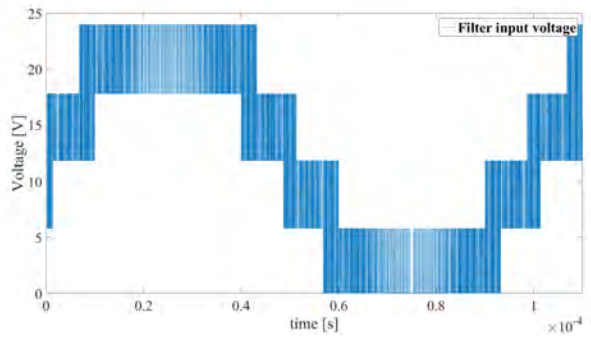

Fig. 9. The modified version of the modulation process, for a sine reference.

IV. Experimental Verification

The performance of the multilevel converter, together with the analog multiplexer, was verified using the sinusoidal test waves. In Figures 10 and 11, 600 kHz and 1.3 MHz sine waves are used as envelope references. Duty-cycle of the multilevel converter is 0.4. It can be seen that multilevel voltage is consisted of stable voltage levels, but with additional voltage spikes due to parasitic resonances. These resonances occurs due to parasitic capacitances and stray inductances of the transistors and finite length lines from the supply voltage to the switching transistors.

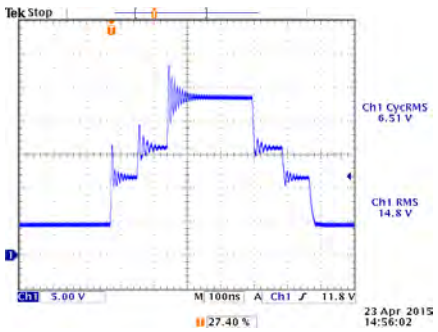

Fig. 10. Analog multiplexer output voltage in the case of a 600 kHz sine wave.

In Figure 12, the verification of whole envelope tracker is presented. The magenta line represents multilevel voltage and the blue line represents amplified envelope signal, in the case of 5 MHz 64QAM signal.

Finally, in Figure 13, the eficiency of the envelope tracker for 5 MHz 64QAM envelope signal is presented, using both Si and GaN based transistors, for different values of duty-cycle of multilevel converter. The switching frequency of multilevel converter is 150 kHz. As can be seen, better efficiency of overall system is reached with GaN based prototype, with peak value of 75%, for the duty-cycle of the multilevel converter about 0.5.

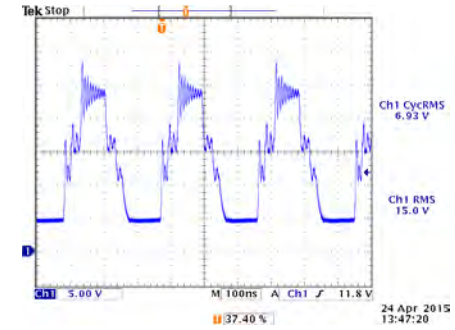

Fig. 11. Analog multiplexer output voltage in the case of a 3.6 MHz sine wave.

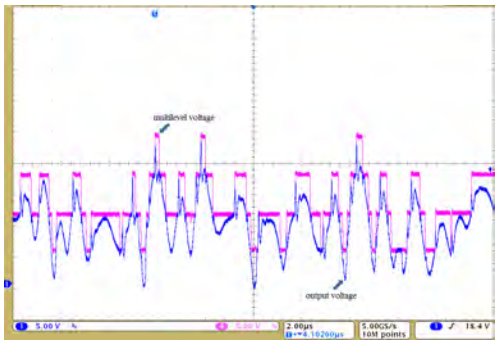

Fig. 12. Analog multiplexer and envelope tracker output voltages in the case of a 5 MHz 64QAM signal.

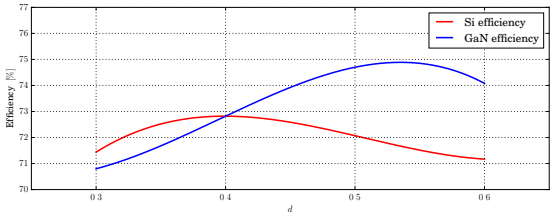

Fig. 13. The efficiencies of envelope amplifier over different duty cycles in the case of a 5 MHz 64QAM signal.

In Figures 14 and 15, 100 kHz and 500 kHz sine waves are used as envelope references for the second proposed EA circuit. The yellow lines represent the input voltage in the filter and the blue lines represent the envelope tracker's output voltage.

At the end, this design was verified by using 2 MHz 64QAM signal reference, which is shown in figure 16. The output power was about 11.5W and the achieved efficiency was about 77%. The efficiency is strongly damaged by driving losses and C_{oss} losses. A modification in this system could be done by replacing diodes with transistors, in that way

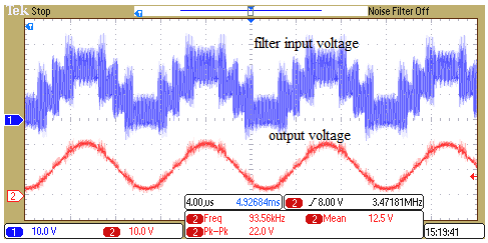

Fig. 14. Filter input and envelope tracker output voltages in the case of a 100 kHz sine wave signal.

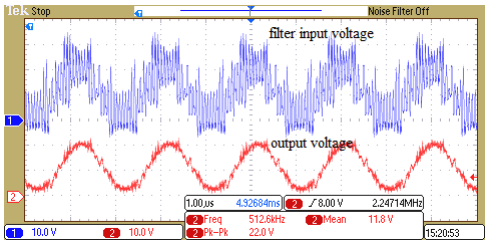

Fig. 15. Filter input and envelope tracker output voltages in the case of a 500 kHz sine wave signal.

giving the oportunity to operate with zero-voltage switching and improving the efficiency.

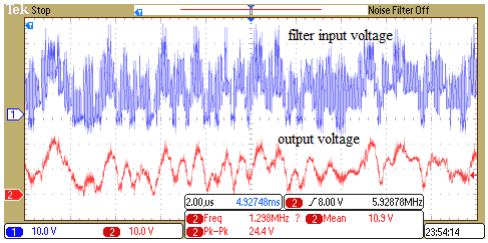

Fig. 16. Filter input and envelope tracker output voltage in the case of a 2 MHz 64QAM signal.

Although the magnitude response of the proposed filters is flat in pass-band, the phase distortion exists and together with the finite switching frequency they produce errors in the output signal. For the better quality and high-fidelity envelope tracking, phase pre-distortion is needed [1].

V. Conclusion and Future Work

In this paper, two different approaches in envelope tracking power supplies are presented. The critical point in this design is envelope tracker's efficiency, due to the increased bandwidth of the transmitted signals. The first approach, with linear assisted switching converter, is proven to provide very accurate tracking for 5 MHz 64QAM envelope reference with peak efficiency of 73% for Si based switches and 75% for GaN based switches. GaN technology is very promising when high efficiency is needed, especially when operating at high frequencies. The main part of the lost power in this approach is caused by linear regulator stage. The second approach, based on high frequency PWM switching, is proven to provide accurate tracking up to 2 MHz 64QAM envelope reference, with the achieved efficiency of 77%. The main disadvantage of this approach are high switching losses (the driving losses and the C_{oss} losses on the transistors), caused with very high switching frequency. The modification in this circuit should be done in order to be able to achieve zero voltage switching. It can be seen that with this technology better efficiency can be achieved with the linear assisted power supply, for the same bandwidth of the 64QAM signal. However, hardware complexity of the linear assisted ET is more evident (DA converter, circuitry for the linear regulator control). On the other hand, five level buck ET has more complex modulation and FPGA with better characteristics is needed (Table II).

TABLE II
The comparison of two envelope trackers

	signal reference	efficiency	system complexity
Linear assisted ET	5 MHz 64QAM	75%	hardware
Five level buck ET	2 MHz 64QAM	77%	digital control

Full comparative analysis of this two approaches is predicted to be done after integrating process with RF PA in order to examine a quality of 64QAM signal processing. It is also projected to quantify impact of the converter switching frequency, duty cycle resolution and transport delays on the output signal quality, using the constellation diagrams and proposed metrics, which are topic for the next paper.

Acknowledgment

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